DUO-MODE KEEPER CIRCUIT

ABSTRACT OF THE DISCLOSURE

LSDL logic is provided with circuitry that has logic controls to provide two modes of operation. The half latch and the PFET that normally forms the keeper function on the dynamic node are modified. The inverter function of the series connected PFET and NFET have their corresponding positive and negative power supply terminals coupled to logic gates. In this way, the inverter may be turned ON so that the half latch functions as a keeper or it may be turned OFF to remove it from operating at all in the mode where the LSDL logic circuit needs to operate with a fast pulse clock. Likewise, the positive supply voltage may be removed while allowing the NFET device to operate to turn ON the PFET pull-up device for burn-in operation.